SUPPRESSION OF CHEMICAL REACTIVITY ON SEMICONDUCTOR SURFACES

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation-in-part of U.S. Patent Application 10/377,015, filed on February 28, 2003, herein incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] The present invention relates to improvements for semiconductors, and particularly to compositions, kits, and preparations for providing a passivated semiconductor surface free of dangling bonds and free of strained bonds.

[0003] Dangling bonds and strained bonds are an inherent nature of semiconductor surfaces. Dangling and strained bonds cause a variety of problems in the fabrication of solid-state devices on semiconductor substrates. They are responsible for the high chemical reactivity of the surface by acting as reaction sites for chemical reactions and create surface states that cause the observed properties of electronic devices to vary from their design specifications. On a semiconductor surface, dangling bonds adsorb oxygen, water, or carbon dioxide, and a layer of native oxide is formed as soon as the surface is exposed to air. Thus, there remains a need to create a passivated semiconductor surface free of dangling bonds and free of strained bonds

[0004] Traditionally, the passivation of semiconductor surfaces has been realized with a thin layer of a dielectric, such as silicon dioxide (SiO_2) or silicon nitride (Si_3N_4) prepared by oxidation, chemical vapor deposition or physical vapor deposition. Unfortunately, the thickness of the passivation layer is typically a few nanometer (nm) to a few micrometers (μm). As such, the semiconductor surface covered with a dielectric of such a thickness no longer behaves as a semiconducting surface, but an insulating one. Thus, there remains a need to passivate such a surface without changing the conducting nature of the surface.

[0005] Other methods that have been used over the years to attempt to reduce or passivate surface states on semiconductor substrates often impede the ability of solid-state devices to behave as they are designed. For example, an alternative method to passivate semiconductor surfaces, hydrogen passivation, often breaks down in air after a short period of time (minutes). This method relies on converting semiconductor-hydrogen bonds from dangling semiconductor bonds, but suffers from steric problems due to the fact that there is insufficient room to break up the dimer bonds and fully hydrogenate the silicon (100) surface. As a result, there are still surface effects that detract from the performance of any semiconductor devices ultimately formed on such a substrate.

[0006] With such problems, no current methods effectively suppress silicidation between silicon and metals or suppress surface oxidation on silicon. Therefore, there exists a need for an effective method of passivating a semiconductor while concomitantly minimizing any carry over effects from the passivation itself.

SUMMARY OF THE INVENTION

[0007] The present invention provides for a passivated semiconductor surface free of dangling bonds and free of strained bonds. With the present invention the chemical reactivity of the surface is suppressed. Because the thickness of the passivation layer is precisely controlled (generally to one atomic layer, equivalent to at least about one Angstrom thick), the passivated surface is capable of keeping its semiconducting nature.

[0008] In one form, the present invention is a method of preventing interfacial reactions between a semiconductor surface and a metal or dielectric comprising the steps of preparing a passivated semiconductor surface using a valence-mending agent and depositing a layer of metal or depositing a dielectric or dielectric precursor on the valence-mended semiconductor surface. The metal is generally selected from those used with semiconductor devices and the dielectric or dielectric precursor may be one that exhibits a high dielectric constant, k, larger than 4. As used herein, a semiconductor surface may be selected from those known to one of ordinary skill in the art, wherein at least one surface is available for preparation and deposition. Similarly, as used herein, a passivating agent is generally a

Group VI congener (element), but may include congeners from other Groups. In addition, as used herein, a valence-mended semiconductor surface is one atomic layer thick.

[0009] In another form, the present invention is a method of suppressing chemical reactions on a semiconductor surface comprising the steps of preparing a passivated semiconductor surface using a valence-mending agent and suppressing chemical reactions from occurring on the valence-mended semiconductor surface even when it is heated. The method prevents adsorbates that weakly bond to the valence-mended semiconductor surface prior to heating from bonding after heating, such that they desorb with heating. Heating temperatures may include ranges of at least about 100 to 600 degrees Centigrade.

[0010] In still another form, the present invention is a method of cleaning a semiconductor surface and/or preventing oxidation on the surface comprising the steps of preparing a passivated semiconductor surface using a valence-mending agent and heating the valence-mended semiconductor surface. Heating cleans the surface without oxidation.

[0011] Still another form of the present invention provides a semiconductor surface free of interfacial reactions between the surface and a second molecular species comprising a semiconductor surface with one atomic layer of valence-mending agents, wherein valence mending occurs after introducing the semiconductor surface to a passivating agent. Generally, the second molecular species is one that may be deposited or forms on the surface, including metals, dielectrics, and reactants, such as oxygen, water vapor, carbon, hydrogen, carbon dioxide, carbon monoxide, and combinations thereof. Interfacial reactions may be those that interfere with the semiconductor surface, including oxidation, degradation, condensation, vaporization, adsorption, silicidation, and combinations, thereof.

[0012] The present invention also provides for a kit for preventing interfacial reactions from occurring on a semiconductor surface comprising a passivating agent and an instructional manual.

[0013] One advantage of the present invention is that the passivation layer formed by the passivating agent is small enough (often about one Angstrom thick) that the semiconductor surface still provides semiconducting behaviors. As presented herein, the

passivation is a monolayer that saturates all the dangling bonds and relaxes all the strained bonds on the semiconductor surface such that the surface becomes much less reactive chemically. With the present invention, the passivated semiconductor surface, when in contact with various reactants (e.g., oxygen, water vapor, metals, metal oxides, etc.) suppresses such reactants from reacting with the surface.

[0014] Those skilled in the art will further appreciate the above-noted features and advantages of the invention together with other important aspects thereof upon reading the detailed description that follows in conjunction with the drawings.

BRIEF DESCRIPTION OF THE FIGURES

[0015] For more complete understanding of the features and advantages of the present invention, reference is now made to the detailed description of the invention along with the accompanying FIGURES, wherein:

FIGURE 1 depicts the atomic structure of a nascent silicon (100) surface with (A) side view into the [011] direction and (B) top view into the [100] direction, wherein dark circles are surface atoms, open circles are second-layer atoms, third, fourth, and fifth layer atoms are gray circles, and each surface atom has two dangling bonds;

FIGURE 2 depicts a side view into the [011] direction of (A) a reconstructed silicon (100) surface and (B) a Group VI-passivated silicon (100) surface, wherein dark circles represent surface silicon atoms, white circles are second layer atoms and gray circles are bulk atoms;

FIGURE 3 depicts the atomic structure of a valence-mended silicon (100) surface with a monolayer of sulfur, selenium, or tellurium with (A) side view into the [011] direction and (B) top view into the [100] direction, wherein hatched circles are Group VI atoms and the passivated surface has no dangling bonds;

FIGURE 4 depicts the phase behavior of sulfur selenium and tellurium as a function of temperature and pressure;

FIGURE 5 depicts transmission electron micrographs of interfaces between nickel and silicon (100) annealed at different temperatures, including (A) bare silicon (100) with nickel annealed at 400 degrees Centigrade, (B) bare silicon (100) with nickel annealed at 500 degrees Centigrade, (C) selenium-passivated silicon (100) with nickel annealed at 500 degrees Centigrade, and (D) selenium-passivated silicon (100) with nickel annealed at 600 degrees Centigrade;

FIGURE 6 depicts an observed pressure of selenium during the passivation of silicon (100) by molecular beam epitaxy in accordance with the present invention;

FIGURE 7 depicts a current-voltage characteristic of (a) as-deposited magnesium contacts and (b) annealed magnesium contacts at 300 degrees Centigrade in an nitrogen ambient for 30 seconds;

FIGURE 8 is a band diagram of magnesium-silicon contacts (A) without interface states and (b) with interface states; and

FIGURE 9 is a rectification ratio (I_f/I_r at V=±0.3 V) as a function of annealing temperature for magnesium contacts on hydrogen-passivated and selenium-passivated silicon (100).

DETAILED DESCRIPTION OF THE INVENTION

[0016] The invention, as defined by the claims, may be better understood by reference to the following detailed description. The description is meant to be read with reference to the FIGUREs contained herein. This detailed description relates to examples of the claimed subject matter for illustrative purposes, and is in no way meant to limit the scope of the invention. The specific aspects and embodiments discussed herein are merely illustrative of ways to make and use the invention, and do not limit the scope of the invention.

[0017] A semiconductor surface is where chemical bonds are broken and dangling bonds are created. For example, each surface atom on the (100) surface of silicon has two dangling bonds, as shown in FIGURE 1, which make the surface chemically reactive. When the surface is exposed to air, the dangling bonds quickly react with air and chemically adsorb molecules or species from the air: water (H_2O), carbon dioxide (CO_2), oxygen (O_2), etc.

When the surface is in contact with other materials such as metals or metal oxides, interfacial reactions take place, which form an interfacial layer of silicide or oxide with or without heating.

[0018] When a clean silicon (100) surface is kept in ultrahigh vacuum, it has little chance for adsorption or reaction with external species. Under such conditions, the surface undergoes reconstruction to reduce its energy. Each atom on a reconstructed silicon (100):2×1 surface has one dangling bond and shares a dimer bond with a neighboring surface atom, as shown in FIGURE 2(a). Electrically, surface states originate from dangling bonds and strained surface bonds (i.e., dimer bonds and back bonds) and often pin the surface Fermi level, causing surface band bending. When a metal is deposited on the silicon (100) surface, surface states (now more appropriately, interface states) pin the interface Fermi level, making the Schottky barrier height less dependent on metal work function and semiconductor electron affinity and instead, the barrier height is controlled by surface states.

[0019] To eliminate dangling bonds on semiconductor surfaces, the present invention provides for a method of preparing a very thin layer of valence-mending atoms on a semiconductor surface. In one embodiment, the thin layer is precisely one atomic layer. For a silicon (100) surface, valence-mending atoms include most of the Group-VI elements, such as sulfur (S), selenium (Se), and tellurium (Te). An example of the atomic structure of a valence-mended silicon (100) surface is shown in FIGURE 3.

[0020] The concept of "valence-mending" was proposed to eliminate dangling bonds on semiconductor surfaces. For the silicon (100) surface, valence-mending atoms include Group VI atoms sulfur (S), selenium (Se) and tellurium (Te). They can bridge between two surface atoms and nicely terminate dangling bonds and relax strained bonds on silicon (100), as shown in FIGURE 2(b). This structure is often noted as a 1×1 reconstruction. The difficulty with valence mending is controlling the amount of passivating agent that is incorporated so that a new layer of material that significantly interferes with the intrinsic properties of the semiconductor substrate is not built up.

[0021] Today, 95% of all semiconductor devices are field effect transistors (FETs). These are not the transistors, however, that Bardeen first demonstrated in 1947. The first example of a solid-state device was a point contact transistor that was less subject to the problems inherent in the formation of an FET. The difficulty in preparing an FET arose from problems caused by surface effects or surface states in the semiconductor material. The surface states were a direct result of dangling bonds on the surface of the semiconductor.

[0022] The present invention provides, for example, a method for passivating the surface of a semiconductor without substantially altering the properties of the underlying material. As a result, solid-state devices that have been passivated in accordance with the present invention display greatly lowered Schottky barriers, or alternatively, improved ohmic contacts. Before the use of the present invention, no metal-semiconductor interface has been observed to have a Schottky barrier of less than 0.4 electron volts on n-type silicon. For example, the reported Schottky barrier value of aluminum-silicon contacts is 0.7 electron volts. This is contrasted with the aluminum-silicon contacts in accordance with the present invention that exhibit Schottky barriers of 0.06 to 0.1 electron volts, values much closer to the theoretical value of –0.01 than previously observed. Similarly, chromium-silicon contacts have been reported to have Schottky barriers of 0.61 electron volts. When Cr-Si contacts are prepared in accordance with the present invention the observed barrier is 0.25 electron volts, which is very close to the theoretical barrier height of 0.21 electron volts.

[0023] The present invention may also be used to prepare ohmic contacts, i.e., a metal- semiconductor contact, with a negative Schottky barrier, or put another way, no Schottky barrier at all. Both magnesium and titanium contacts with silicon have been reported to display Schottky barriers. When these contacts are prepared on surfaces that have been passivated in accordance with the present invention, they become ohmic, i.e., they display no barriers. This is demonstrative of the powerful effects of surface states and the desirability of removing such states from surfaces on which solid-state devices are constructed.

[0024] The present invention involves the application of a passivating agent, also referred to as a passivant, under conditions that allow the passivant to react with a

semiconductor surface but not to agglomerate or otherwise condense to form a thicker layer. In one form, this is accomplished by adjusting the temperature and pressure such that the partial pressure of the passivating agent is below the pressure at which it can condense. Under these conditions the passivant may react when it actually contacts the semiconductor substrate and in so doing forms a monolayer of material across the surface. Once the monolayer is complete no further deposition may take place. Since condensation is also precluded, the substrate may only exist in a monolayer passivated form.

[0025] The present invention may be used with a variety of passivants of varying valence. For example, the congeners of Groups VI in the periodic table may be used to passivate the silicon (100) surface by bridging between surface atoms and eliminating dangling bonds, dimer bonds and strained back bonds. For other semiconductor surface morphologies such as atomic steps, monovalent materials such as halogens of Group VII and hydrogen and its isotopes may be used to passivate those areas of the semiconductor surface.

[0026] FIGURE 4 depicts the known condensation behavior of the Group VI elements, sulfur, selenium and tellurium as a function of pressure and temperature. The line for each element indicates where the condensed and vapor states of the element are in equilibrium with one another. Under conditions to the left of a chosen line in the plot, condensation will occur, and to the right of the same line, the element exists only in its vapor state. The present invention makes use of this data by using conditions where the element only exits in the vapor phase and allowing it to interact with a semiconductor substrate. The gaseous element may only be permanently removed from the vapor phase by contacting the surface and reacting with it. This is how monolayer passivation is accomplished.

[0027] The present invention also provides for methods of suppressing the chemical reactivity of a semiconductor surface by eliminating dangling bonds on the surface. As presented herein, this is achieved by passivating one or more dangling bonds with a very thin layer of valence-mending atoms deposited onto the surface. In one embodiment, the thin layer (e.g., monolayer) is precisely one atomic layer.

Suppression of Reactions Between Semiconductors and Metals

[0028] When a layer of metal is deposited onto a semiconductor surface, interfacial reactions occur and a compound layer (in this case, the semiconductor is silicon and the compound is a silicide) is formed between metal and semiconductor. This can occur with and without heating, often depending on the reactivity of the particular metal/semiconductor pair. With the present invention, when a layer of metal is deposited onto a valence-mended semiconductor surface, interfacial reactions are suppressed up to a higher temperature and no compound is formed below that temperature.

[0029] Deposited metals may include, but are not limited to, titanium, cobalt, nickel, tungsten, molybdenum, platinum, gold, and chromium, of which many are metals commonly used in semiconductor devices. As described, when such metals are in contact with silicon, silicides of different phases and different stoichiometry are formed at the interface (with or without heating). Because silicides may degrade device performance, they are sometimes unwanted. By passivating the semiconductor surface with the method described herein before placing the surface in contact with a metal, interfacial silicide formation is suppressed.

Example of a Suppressed Reaction

[0030] As shown in FIGURE 5A, nickel reacts with a silicon (100) surface when heated to 400 degrees Centigrade and forms both nickel subsilicide (Ni_2Si) and nickel monosilicide (NiSi). When nickel is in contact with a selenium-passivated silicon (100) surface (FIGURE 5C), it resists the formation of either nickel subsilicide or nickel monosilicide when heated to 500 degrees Centigrade. When heated to 600 degrees Centigrade, nickel eventually reacts with the selenium-passivated silicon (100) surface and forms nickel monosilicide, as shown in FIGURE 5D. Nickel subsilicide (reactant) was not observed with contacts between nickel and selenium-passivated silicon (100) at temperature ranges of at least about 300–700 degrees Centigrade. Thus, nickel subsilicide (Ni_2Si) formation was suppressed and nickel monosilicide (NiSi) was the existent phase between nickel and passivated silicon at temperatures between at least about 300-700 degrees Centigrade. As such, the present invention is capably of suppressing the formation of silicides.

Suppression of Reactions Between Semiconductors and Dielectrics

[0031] When a layer of dielectric is deposited onto a semiconductor surface, interfacial reactions often occur, which form a compound between the semiconductor and the dielectric. This compound is sandwiched between the semiconductor and the dielectric, and often degrades the dielectric/semiconductor interface. With the present invention, when a layer of dielectric is deposited onto a valence-mended semiconductor surface, interfacial reactions just described were suppressed. Therefore, by passivating the semiconductor surface with the method described herein before putting the surface in contact with dielectrics, the formation of an interfacial compound is suppressed. The suppression generally occurs at a range of temperatures, such that an interfacial compound is not formed within this temperature range. For example, between hafnium dioxide (HFO_2) and silicon, the selenium-passivated silicon (100) surface can withstand temperatures up to 450 degrees Centigrade.

Example of a Suppressed Interfacial Reaction

[0032] Several dielectric materials with high dielectric constants (the so-called high-k dielectrics, with k (dielectric constant) larger than 4 are thought to be useful for next-generation complimentary metal-oxide-semiconductor (CMOS) devices. These materials include hafnium dioxide (HfO_2), zirconium dioxide (ZrO_2), and their silicates and aluminates, as examples. These materials will replace current dielectrics in CMOS devices, such as silicon dioxide (SiO_2) or silicon oxynitride (SiO_xN_y), compounds that have lower dielectric constants ($k \sim 4$).

[0033] A common problem for these high-k dielectrics when deposited onto a silicon surface is the occurrence of interfacial reactions between silicon and high-k dielectrics. The interfacial reaction generally forms an interfacial oxide layer with a lower dielectric constant. The low-k dielectric defeats the very purpose of utilizing high-k dielectrics. With the present invention, the deposit of a high-k dielectric on a valence-mended silicon surface suppressed the formation of interfacial oxide and a thin high-k dielectric layer was obtained. We have prepared a high-k dielectric, hafnium dioxide, on selenium-passivated silicon (100) and heated it to 600 degrees Centigrade. Electrical measures proved that there were no interfacial

reactions between the dielectric and silicon up to 400 degrees Centigrade. As a comparison, hafnium dioxide was also prepared on non-passivated silicon (100) and interfacial reactions were observed at 200-300 degrees Centigrade.

Suppression of Chemical Reactions on Semiconductor Surfaces

[0034] The present invention is also used to illustrate that a valence-mended semiconductor surface suppresses chemical reactions on that surface. When a bare semiconductor surface is exposed to air, it chemically adsorbs various species in air: oxygen (O_2), carbon dioxide (CO_2), carbon monoxide (CO), water vapor (H_2O), etc. After adsorption, the semiconductor surface is covered with a thin layer of adsorbates that consist of species such as oxygen and carbon.

[0035] With the present invention, a valence-mended semiconductor surface has no dangling bonds on the surface. When such a valence-mended semiconductor surface is exposed to air, it physically adsorbs various species in air; however, the physical adsorbates are only weakly bonded to such a surface. Upon heating of this surface, even at relatively low temperatures of at least about 100–500 degrees Centigrade, the physical adsorbates were found to desorb and the surface was clean from carbon and oxygen. In comparison, chemical adsorbates (such as occurs with non-valence-mended semiconductor surfaces) required much higher temperatures to desorb.

[0036] The above shows that when a passivated silicon surface is exposed to air, chemical adsorption is suppressed and only physical adsorption is present on the surface. This physical adsorption is desorbed by heating the surface to relatively low temperatures (at least about 100–500 degrees Centigrade) and a clean silicon surface is obtained without high-temperature heating (e.g., above 600 degrees Centigrade).

Example of Maintaining a Clean Silicon Surface

[0037] Common adsorbates on a silicon (100) surface include oxygen and carbon. On a selenium-passivated silicon (100) surface, physically adsorbed oxygen and carbon were desorbed by heating the surface to a relatively low temperature, often below a temperature of

at least about 500 degrees Centigrade. On a bare silicon (100) surface, chemically adsorbed oxygen and carbon required a much higher temperature to desorb, often above 900 degrees Centigrade.

[0038] Therefore, a passivated silicon surface when exposed to oxygen or water vapor at elevated temperatures does not lead to the formation of SiO_2 (it is suppressed such that the surface remains free of SiO_2). This is contrasted to a non-passivated or normal silicon surface that will have SiO_2 on its surface after a similar exposure to oxygen or water vapor.

Example of Preventing a Silicon Surface from Oxidation

[0039] When a bare silicon surface was exposed to oxygen or water vapor at elevated temperatures, i.e., above room temperature, a thin layer of silicon dioxide (SiO_2) was formed on the surface. When a valence-mended silicon surface was exposed to oxygen or water vapor at elevated temperatures, the formation of SiO_2 was suppressed and the surface remained free of SiO_2. This suppression generally occurred up to a certain temperature, about 500 degrees Centigrade.

[0040] The present invention reveals several methods of reducing chemical reactivity of semiconductor surfaces. Such methods have numerous applications, such as (a) the suppression of interfacial reactions between silicon and dielectrics with high dielectric constants; (b) the suppression of interfacial reactions between silicon and metals, and (c) the suppression of surface reactions on semiconductor surfaces. The present invention also provides for a method that keeps a semiconductor surface clean.

Preparative Examples of Valence Mending

[0041] Various features of the present invention take advantage of a method of preparing a monolayer of valence-mending atoms on a semiconductor surface. Generally, the monolayer is precisely one atomic layer. Examples are provided for a metal/silicon (100) interface with a monolayer of selenium. As described herein, low Shottky barriers were obtained on n-type silicon (100), and a negative Schottky barrier was demonstrated on n-type silicon (100) with a metal, such as magnesium or titanium.

[0042] FIGURE 6 graphically depicts a passivant reacting with a semiconductor surface until all of the reaction sites on the surface are passivated. With a molecular beam epitaxy (MBE) system, the shutter to a selenium source was opened at time 0 in the plot. The pressure of selenium in the reaction chamber remained low for approximately 60 seconds, indicating that the selenium was reacting with the surface and not building up in the reactor. At approximately 60 seconds, there was a spike in selenium pressure indicating that all of the reactive site on the surface of the silicon (100) wafer were passivated, and all additional selenium that was added was merely surplus and building up as a gas in the reaction chamber.

[0043] N-type silicon (100) wafers were used with antimony doping levels in the low 10^{15} cm^{-3}. The nominal wafer miscut was less than 0.5 degrees. The selenium passivation experiments were performed in two molecular beam epitaxy (MBE) systems connected through an ultrahigh vacuum transfer tube. One of them was for silicon growth and the other for selenium passivation. The wafers were cleaned in 2% hydrofluoric acid for 30 seconds before loaded into the silicon MBE system. Silicon buffer layers of 500 Å with residual antimony doping levels of mid-10^{14} cm^{-3} were grown at about 600 degrees Centigrade and then annealed at about 800 degrees Centigrade for 1 hour. Sharp 2×1 reconstruction was always obtained with reflection high-energy electron diffraction after annealing. Some wafers were unloaded after silicon buffer growth. Other wafers were transferred to the selenium MBE system for passivation. The selenium source temperature was about 224 degrees Centigrade, the passivation time was 60 seconds, and the silicon wafer temperature was 300 degrees Centigrade. Under the conditions described, precisely one monolayer of selenium was deposited on the silicon (100) surface.

[0044] After passivation, metal-silicon contacts were fabricated by electron-beam evaporation and lift-off on selenium-passivated wafers without any cleaning. The metal (such as magnesium) dots were approximately 290 μm in diameter. Metal-silicon contacts were also fabricated on silicon wafers with 500 Å silicon buffer but without selenium passivation. Heating of the metal-silicon contacts was performed with rapid thermal annealing and hot plate.

[0045] Magnesium is known to form a Schottky contact with n-type silicon (100) with a barrier height of 0.4 eV. FIGURE 7(a) shows the current-voltage (I-V) characteristics of magnesium contacts on hydrogen-passivated and selenium-passivated silicon (100), without heating, both of which behave in an ohmic fashion. In fact, ohmic behavior is observed for magnesium contacts on hydrogen-passivated and selenium-passivated silicon (100) with n-type doping levels from low 10^{14} cm^{-3} to high 10^{18} cm^{-3}.

[0046] The work function, ϕ, of magnesium is 3.66 eV, and the electron affinity, χ, of silicon is 4.05 eV. The ideal Schottky barrier height, ϕ_B, for a magnesium-silicon contact free of interface states is $\phi_B = \phi - \chi$, which results in a negative barrier height of -0.39 eV. The negative sign simply means that there is no energy barrier between magnesium and silicon, as shown in FIGURE 8(a). In reality, interface states often pin the interface Fermi level, consistent with the band diagram in FIGURE 8(b). Several metals, including most of the Groups I and II elements, can have the band diagram shown in FIGURE 8(a) with silicon, if only their work functions are considered. However, interface states are so dominant between these materials and silicon that such behavior is typically not observed.

[0047] Ohmic behavior is expected for the band diagram in FIGURE 8(a). For electrons drifting from magnesium-silicon in FIGURE 8(a), there is a small energy hump that is typically less than a few tenths of an electron volt. Once the applied voltage exceeds it, the contact becomes completely ohmic. In many cases, they behave perfectly ohmic.

[0048] Ohmic behavior is also observed for magnesium contacts on hydrogen-passivated silicon (100), as shown in FIGURE 7(a). It is believed that hydrogen passivation also reduces surface states and produces the band diagram in FIGURE 8(a).

[0049] The behavior of these samples after heating is noteworthy. FIGURE 7(b) shows the I-V characteristics of magnesium contacts on hydrogen-passivated and selenium-passivated silicon (100) after rapid thermal annealing at 300 degrees Centigrade for 30 seconds in a nitrogen ambient. While the selenium-passivated sample remains ohmic, the hydrogen-passivated sample turns into a Schottky contact. Selenium passivation produces a

more stable surface than hydrogen passivation. This is significant because a number of heating steps are often required in the manufacture of complex semiconductor devices.

[0050] A first-principle analysis of surface energetics, accomplished by counting dangling bonds and taking into account bond dissociation energies, indicates that the selenium-passivated silicon (100) surface in FIGURE 2(b) is 2.1×10^{-4} cal/cm^2 lower in energy than the hydrogen-passivated silicon (100):2×1 surface. It is likely that hydrogen passivation breaks down and magnesium reacts with silicon to form magnesium silicide at 300 degrees Centigrade. A Schottky contact is then formed between silicon and magnesium silicide. For the selenium-passivated sample, silicide formation is suppressed and the interface remains a magnesium-silicon one at 300 degrees Centigrade.

[0051] To quantify the transition from ohmic to Schottky, the rectification ratio, i.e., the ratio of the forward current, I_f, at forward voltage V_f=0.3 V and the reverse current, I_r, at reverse voltage V_r=-0.3 V is plotted as a function of hot-plate annealing temperature in FIGURE 9 for both hydrogen-passivated and selenium-passivated silicon (100) samples. On these samples the magnesium contacts are capped with 500 Å nickel (Ni) to prevent magnesium oxidation during heating. The ratio for hydrogen-passivated samples starts to rise rapidly from ~1 at ~225 degrees Centigrade (500 K) and saturates to ~40 at ~325 degrees Centigrade (600 K). For the selenium-passivated sample, the ratio stays at ~1 even at 375 degrees Centigrade (650 K). Annealing above 375 degrees Centigrade is difficult because even the nickel-magnesium contacts get oxidized above that temperature. It is believed that, when the annealing temperature is high enough, magnesium and selenium-passivated silicon (100) will eventually react to form magnesium silicide, and its rectification ratio will eventually increase to a value comparable to 40. If the middle point of the rectification ratio, 20, is defined as the transition temperature from ohmic to Schottky, selenium-passivated silicon (100) has a transition temperature that is more than 100 degrees Centigrade higher than that of hydrogen-passivated silicon (100) in FIGURE 9. However, the same characterization has been performed on multiple samples, and the statistics indicates that the transition temperature for hydrogen-passivated samples are consistently between 275–300 degrees Centigrade, and that temperature for selenium-passivated samples fluctuates from 300 degrees Centigrade to above 375 degrees Centigrade.

[0052] In one form, a method for passivating a semiconductor surface with a thin layer or monolayer of a passivating agent (capable of providing valence-mending atoms) includes the steps of placing a semiconductor substrate, having at least one surface in a chamber, and heating the semiconductor substrate to a temperature. The semiconductor substrate is then exposed to a passivating agent for a period of time sufficient to react with substantially all of the surface, and the partial pressure of the passivating agent is such that the passivating agent will not condense at the temperature of the substrate. As a result of this treatment the presence of surface states is greatly reduced and one atomic layer of valence-mending atoms is formed on the semiconductor surface.

[0053] In another form, a method for manufacture of a semiconductor device with a low Schottky barrier includes the steps of placing an p-type semiconductor substrate having at least one surface in a chamber and heating the semiconductor substrate to a temperature. The semiconductor substrate is then exposed to a passivating agent (capable of providing valence-mending atoms) for a period of time sufficient to react with substantially all of the surface, and the partial pressure of the passivating agent is such that the passivating agent will not condense at the temperature of the substrate. As a result of this treatment the presence of surface states is greatly reduced and one atomic layer of valence-mending atoms is formed on the semiconductor surface. A portion of the semiconductor surface is then metallized with a metal having a work function whose magnitude is slightly greater than the magnitude of the electron affinity and the band gap of the p-type semiconductor substrate.

[0054] In still another form, a method for manufacture of a semiconductor device with a low Schottky barrier includes the steps of placing a p-type semiconductor substrate having at least one surface in a chamber and heating the semiconductor substrate to a temperature. The semiconductor substrate is then exposed to a passivating agent (capable of providing valence-mending atoms) for a period of time sufficient to react with substantially all of the surface, and the partial pressure of the passivating agent is such that the passivating agent will not condense at the temperature of the substrate. As a result of this treatment the presence of surface states is greatly reduced and one atomic layer of valence-pending atoms is formed on the semiconductor surface. A portion of the semiconductor surface is then metallized with a metal having a work function whose magnitude is slightly less than the sum

of the magnitude of the electron affinity and the band gap of the p-type semiconductor substrate.

[0055] In still another form, a method for manufacture of a semiconductor device with improved ohmic contacts comprises the steps of placing an n-type semiconductor substrate having at least one surface in a chamber and heating the semiconductor substrate to a temperature. The semiconductor substrate is then exposed to a passivating agent (capable of providing valence-mending atoms) for a period of time sufficient to react with substantially all of the surface, and the partial pressure of the passivating agent is such that the passivating agent will not condense at the temperature of the substrate. As a result of this treatment the presence of surface states is greatly reduced and one atomic layer of valence-mending atoms is formed on the semiconductor surface. A portion of the semiconductor surface is then metallized with a metal having a work function whose magnitude is less than the magnitude of the electron affinity of the n-type semiconductor substrate.

[0056] In yet another form, a method for manufacture of a semiconductor device with improved ohmic contacts includes the steps of placing a p-type semiconductor substrate having at least one surface in a chamber and heating the semiconductor substrate to a temperature. The semiconductor substrate is exposed to a passivating agent (capable of providing valence-mending atoms) for a period of time sufficient to react with substantially all of the surface, and the partial pressure of the passivating agent is such that the passivating agent will not condense at the temperature of the substrate. As a result of this treatment the presence of surface states is greatly reduced and one atomic layer of valence-mending atoms is formed on the semiconductor surface. A portion of the semiconductor surface is then metallized with a metal having a work function whose magnitude is greater than the sum of the magnitude of the electron affinity and the band gap of the p-type semiconductor substrate.

[0057] While specific alternatives to steps of the invention have been described herein, additional alternatives not specifically disclosed but known in the art are intended to fall within the scope of the invention. Thus, it is understood that other applications of the present invention will be apparent to those skilled in the art upon reading the described embodiment and after consideration of the appended claims and drawing.